

## Claims

- 5     1.     A computer system including:  
         a processor;  
         a controller;  
         a data communications facility interconnecting said processor and  
controller; and  
10           a memory having a plurality of locations for storing data;  
         wherein said controller is responsive to a single command received  
from the processor to copy data from a first memory location to a second  
memory location, wherein said single command specifies said first and second  
memory locations.
- 15           2.     The system of claim 1, wherein said memory is coupled to said data  
communications facility via a memory controller.
3.     The system of claim 2, wherein the data is copied from the first  
20     memory location to the second memory location by an internal memory  
transfer, without travelling over the data communications facility.
4.     The system of claim 2, wherein said controller is provided by said  
memory controller.
- 25           5.     The system of claim 1, wherein a first portion of memory is coupled to  
said data communications facility via a first memory controller and includes  
said first memory location, and a second portion of memory is coupled to said

data communications facility via a second memory controller and includes said second memory location.

6. The system of claim 5, wherein the data is copied from the first  
5 memory location to the second memory location by using a peer-to-peer copy operation on the data communication facility.

7. The system of claim 6, wherein said data communications facility  
supports direct memory access (DMA), and said peer-to-peer copy operation  
10 is performed by using a transaction analogous to DMA.

8. The system of claim 5, wherein said controller is provided by said first and second memory controllers.

15 9. The system of claim 1, wherein the controller maintains a record of copy operations that are currently in progress.

10. The system of claim 1, wherein the processor is allowed to continue processing operations prior to completion of the copy.

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11. The system of claim 10, wherein the controller redirects a read request for the second memory location to the first memory location if the copy has not yet completed.

25 12. The system of claim 10, wherein the controller delays a write request for the first memory location pending completion of the copy.

13. The system of claim 10, wherein in response to a write request for the second memory location prior to completion of the copy, the controller cancels completion of the copy for the part of the second memory location subject to the write request.
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14. The system of claim 1, further comprising a cache, and wherein any cache entry for the second memory location is invalidated in response to said single command.
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15. The system of claim 14, wherein any cache entry for the second memory location is invalidated by the processor.
16. The system of claim 14, wherein any updated cache entry for the first memory location is flushed to memory in response to said single command.
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17. The system of claim 1, wherein said processor supports a specific programming command to copy data from a first memory location to a second memory location.
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18. The system of claim 1, wherein said data communications facility is a bus.
19. The system of claim 18, wherein said bus supports a command set, and said single command is part of said command set.
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20. The system of claim 1, wherein said controller transmits an acknowledgement of said single command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement

within a predetermined time-out period to perform said copy operation by issuing separate read and write commands.

21. A computer system including:
- 5 processor means;  
controller means;  
data communications means for interconnecting said processor means and said controller means; and  
memory means having a plurality of locations for storing data;
- 10 wherein said controller means includes means responsive to a single command received from the processor means for copying data from a first memory location to a second memory location, wherein said single command specifies said first and second memory locations.
- 15 22. A method for operating a computer system including a processor, a controller, a data communications facility interconnecting said processor and controller, and a memory having a plurality of locations for storing data, said method comprising:
- issuing a single command from the processor to the controller, said  
20 command specifying a first memory location and a second memory location;  
and  
responsive to receipt of said single command by the controller,  
copying data from a first memory location to a second memory location.
- 25 23. The method of claim 22, wherein said data communications facility is a bus that supports a command set, and said single command is part of said command set.

24. The method of claim 22, wherein the data is copied from the first memory location to the second memory location by an internal memory transfer, without travelling over the data communications facility.
- 5 25. The method of claim 22, wherein the processor is allowed to continue processing operations prior to completion of the copy.
26. The method of claim 25, further comprising redirecting a read request for the second memory location to the first memory location if the copy has  
10 not yet completed.
27. The method of claim 25, further comprising delaying a write request for the first memory location pending completion of the copy.
- 15 28. The method of claim 25, further comprising cancelling completion of the copy for any portion of the second memory location which is subject to a write request prior to completion of the copy.
29. The method of claim 22, wherein the computer system further  
20 comprises a cache, and wherein said method further comprises invalidating any cache entry for the second memory location in response to said single command.
30. The method of claim 29, further comprising flushing any updated  
25 cache entry for the first memory location to memory in response to said single command.